CLAIMS

What is claimed is:

1. A fuse of a semiconductor device, comprising:

a central region disposed directly adjacent an insulative structure of the semiconductor device; and

two terminal regions, a first of said two terminal regions being disposed adjacent a first end of said central region and a second of said two terminal regions being disposed adjacent a second end of said central region, each of said two terminal regions being separated from said insulative structure by a layer of conductive material.

2. The fuse of claim 1, wherein at least said central region comprises a metal silicide.

3. The fuse of claim 1, wherein at least said central region comprises tungsten silicide.

4. The fuse of claim 1, wherein said central region is narrower in width than both of said two terminal regions.

5. The fuse of claim 1, wherein said insulative structure comprises a glass, a silicon oxide, a silicon nitride, or a silicon oxynitride.

6. The fuse of claim 1, wherein said insulative structure comprises a field oxide of the semiconductor device.

7. The fuse of claim 1, wherein said layer of conductive material comprises polysilicon.

8. The fuse of claim 1, wherein each of said two terminal regions and said central region comprise a metal silicide.

9. The fuse of claim 1, wherein each of said two terminal regions and said central region comprise tungsten silicide.

10. The fuse of claim 1, wherein said two terminal regions communicate with one another by means of said central region.

11. The fuse of claim 1, wherein said central region is discontinuous.

12. The fuse of claim 1, further comprising a contact in communication with one of said two terminal regions.

13. The fuse of claim 12, further comprising another contact in communication with another of said two terminal regions.

14. The fuse of claim 1, wherein each of said two terminal regions comprises a greater volume than said central region.

15. The fuse of claim 1, wherein said insulative structure conducts substantially no electrical current.

16. The fuse of claim 1, wherein each of said two terminal regions and said central region have substantially the same resistance.

17. A method of fabricating a fuse upon a semiconductor device, comprising: disposing a layer of conductive material over an insulative structure of the semiconductor device;

patterning said layer of conductive material to define at least two spaced apart regions of conductive material through which said insulative structure is exposed;

disposing a layer of metal silicide over the semiconductor device, including adjacent to said at least two regions and to said insulative structure exposed between said at least two regions; and

patterning said layer of metal silicide so as to define at least two terminal regions of the fuse, each of which ~~are~~ is in contact with a corresponding one of said at least two regions of ~~said layer of~~ conductive material, and a central region disposed between said at least two terminal regions and in contact with said insulative structure.

18. The method of claim 17, wherein said disposing said layer of conductive material comprises disposing polysilicon onto said insulative structure.

19. The method of claim 17, wherein said patterning said layer of conductive material comprises disposing a mask over the semiconductor device and removing selected regions of said layer of conductive material through said mask.

20. The method of claim 19, wherein said disposing said mask comprises:

disposing photoresist onto the semiconductor device;

exposing selected regions of said photoresist; and

developing said selected regions.

21. The method of claim 19, wherein said removing comprises etching selected regions of said layer of conductive material through said mask.

22. The method of claim 21, wherein said etching comprises isotropically etching said selected regions.

23. The method of claim 21, wherein said etching comprises wet etching said selected regions of said layer of conductive material.

24. The method of claim 17, wherein said disposing said layer of conductive material comprises chemical vapor depositing said layer of conductive material.

25. The method of claim 17, wherein said depositing said layer of metal silicide comprises chemical vapor depositing said layer of metal silicide.

26. The method of claim 17, wherein said depositing said layer of metal silicide comprises depositing tungsten silicide.

27. The method of claim 17, wherein said patterning said layer of metal silicide comprises disposing a mask over the semiconductor device and removing selected regions of said layer of metal silicide through said mask.

28. The method of claim 27, wherein said disposing said mask comprises:
disposing photoresist over the semiconductor device;
exposing selected regions of said photoresist; and
developing said selected regions.

29. The method of claim 27, wherein said removing comprises etching said selected regions of said layer of metal silicide.

30. The method of claim 29, wherein said etching comprises anisotropically etching said selected regions of said layer of metal silicide.

31. The method of claim 29, wherein said etching comprises dry etching said selected regions of said layer of metal silicide.

32. The method of claim 17, further comprising disposing a contact in communication with at least one of said at least two terminal regions.

33. The method of claim 32, further comprising disposing another contact in communication with another of said at least two terminal regions.

34. A semiconductor device, comprising:

an insulating substrate;

at least two spaced apart regions of polysilicon disposed over the insulating substrate; and

a metal silicide fuse comprising a central region disposed adjacent the insulating substrate and between said at least two spaced apart regions and at least two terminal regions disposed on said at least two spaced apart regions of polysilicon and on each end of said central region.

35. The semiconductor device of claim 34, wherein said insulating substrate comprises an isolation region.

36. The semiconductor device of claim 35, wherein said isolation region comprises a field oxide.

37. The semiconductor device of claim 36, wherein said field oxide region is disposed on a semiconductor substrate.

38. The semiconductor device of claim 34, wherein said insulating substrate is disposed upon a semiconductor substrate.

39. The semiconductor device of claim 34, further comprising a layer of dielectric material disposed between said metal silicide fuse and said at least two spaced apart polysilicon regions.

40. The semiconductor device of claim 34, wherein a volume of said central region is less than a volume of each of said at least two terminal regions.

41. The semiconductor device of claim 34, wherein said central region is narrower in width than said at least two terminal regions.

42. The semiconductor device of claim 34, wherein said central region is rendered discontinuous when exposed to at least a programming current.

43. The semiconductor device of claim 34, wherein the at least two discrete portions are electrically isolated from each other when said central region is discontinuous.

44. The semiconductor device of claim 34, wherein said at least two spaced apart regions of polysilicon comprises doped polysilicon.

45. The semiconductor device of claim 38, wherein said semiconductor substrate comprises at least two separate diffusion regions therein exposed at a surface thereof.

46. The semiconductor device of claim 45, further comprising at least one gate disposed upon said semiconductor substrate and between two of said at least two separate diffusion regions.

47. The semiconductor device of claim 46, wherein said at least one gate comprises a gate oxide, a polysilicon conductive element disposed on said gate oxide, and a metal silicide element disposed on said polysilicon conductive element.

48. The semiconductor device of claim 47, wherein said polysilicon conductive element is disposed upon the semiconductor device at the same fabrication level as said at least two ~~spaced apart regions~~ discrete portions of polysilicon.

49. The semiconductor device of claim 47, wherein said metal silicide element is disposed upon the semiconductor device at the same fabrication level as said metal silicide fuse.

50. A method of fabricating a fuse, comprising:

fabricating spaced apart regions comprising polysilicon on an insulative structure of a semiconductor device; and

fabricating a fuse comprising a metal silicide, including a central region disposed adjacent the insulative structure and between said spaced apart regions and at least two terminal regions disposed on opposite ends of the central region and adjacent said ~~at least two~~ spaced apart regions.

51. The method of claim 50, wherein said fabricating spaced apart regions comprises:

disposing polysilicon onto said insulative structure; and

patterning said polysilicon.

52. The method of claim 51, wherein said disposing polysilicon comprises chemical vapor depositing polysilicon.

53. The method of claim 51, further comprising doping said polysilicon.

54. The method of claim ~~51~~ 53, wherein said doping occurs substantially simultaneously with said disposing.

55. The method of claim 51, wherein said patterning comprises disposing a mask adjacent said polysilicon and removing selected regions of said polysilicon through said mask.

56. The method of claim 55, wherein said disposing said mask comprises disposing photoresist adjacent said polysilicon, exposing selected regions of said photoresist, and developing said selected regions.

57. The method of claim 55, wherein said removing selected regions of said polysilicon comprises etching said selected regions.

58. The method of claim 57, wherein said etching comprises isotropically etching said selected regions.

59. The method of claim 57, wherein said etching comprises wet etching said selected regions.

60. The method of claim 50, wherein said fabricating said fuse comprises disposing metal silicide adjacent said ~~at least two~~ spaced apart regions and said insulative structure exposed therebetween.

61. The method of claim 60, wherein said disposing metal silicide comprises chemical vapor depositing metal silicide.

62. The method of claim 60, wherein said fabricating said fuse further comprises patterning said metal silicide.

63. The method of claim 62, wherein said patterning comprises disposing a mask adjacent said metal silicide and removing selected regions of said metal silicide through said mask.

64. The method of claim 63, wherein said disposing said mask comprises disposing photoresist adjacent said metal silicide, exposing selected regions of said photoresist, and developing said selected regions.

65. The method of claim 63, wherein said removing selected regions of said metal silicide comprises etching said metal silicide.

66. The method of claim 65, wherein said etching comprises anisotropically etching said selected regions.

67. The method of claim 65, wherein said etching comprises dry etching said selected regions.

68. The method of claim 62, wherein said patterning comprises defining at least two terminal regions of the fuse adjacent said spaced apart regions and a central region of the fuse adjacent said insulative structure.

69. The method of claim 50, further comprising doping said spaced apart regions of polysilicon.

70. The method of claim 69, wherein said doping occurs substantially simultaneously with disposing polysilicon on said insulative structure.

71. A method of substantially simultaneously fabricating a gate and a fuse on a semiconductor substrate, comprising:

disposing a layer of insulative material over at least an exposed region of the semiconductor substrate;

disposing a layer of polysilicon over the semiconductor device, including over said layer of insulative material and over field oxide regions disposed on the semiconductor substrate;

patterning at least regions of said layer of polysilicon disposed on said field oxide regions;

disposing a layer of metal silicide on said layer of polysilicon;

patterning at least said layer of metal silicide to define the fuse and the gate therefrom.

72. The method of claim 71, wherein said disposing said layer of polysilicon comprises chemical vapor depositing said layer of polysilicon.

73. The method of claim 71, wherein said patterning said at least regions comprises defining at least two spaced apart regions of polysilicon on said field oxide region and between which said field oxide region is exposed.

74. The method of claim 73, wherein said defining the fuse comprises defining a central region disposed adjacent and substantially between said at least two spaced apart regions and defining at least two terminal regions, each terminal region continuous with an end of said central region and disposed adjacent one of said at least two spaced apart regions.

75. The method of claim 73, wherein said defining said at least two spaced apart regions comprises disposing a mask over said layer of polysilicon and removing selected regions of said layer of polysilicon through said mask.

76. The method of claim 75, wherein said disposing said mask comprises disposing photoresist over said layer of polysilicon, exposing selected regions of said photoresist, and developing said selected regions.

77. The method of claim 75, wherein said removing comprises etching said layer of polysilicon.

78. The method of claim 77, wherein said etching comprises wet etching said layer of polysilicon.

79. The method of claim 77, wherein said etching comprises isotropically etching said layer of polysilicon.

80. The method of claim 71, further comprising patterning gate regions of said layer of polysilicon.

81. The method of claim 80, wherein said patterning said gate regions occurs substantially simultaneously with said patterning said at least regions of said layer of polysilicon.

82. The method of claim 80, wherein said patterning said gate regions comprises disposing a mask over said layer of polysilicon and removing selected regions of said layer of polysilicon through said mask.

83. The method of claim 82, wherein said disposing said mask comprises disposing photoresist over said layer of polysilicon, exposing selected regions of said layer of polysilicon, and developing said selected regions.

84. The method of claim 82, wherein said removing comprises etching said selected regions.

85. The method of claim 84, wherein said etching comprises dry etching said selected regions.

86. The method of claim 84, wherein said etching comprises anisotropically etching said selected regions.

87. The method of claim 71, wherein said disposing said layer of metal silicide comprises chemical vapor depositing said layer of metal silicide.

88. The method of claim 71, wherein said defining the fuse and the gate from at least said layer of metal silicide comprises disposing a mask over said layer of metal silicide and removing selected regions of said layer of metal silicide through said mask.

89. The method of claim 88, wherein said disposing said mask comprises disposing photoresist over said layer of metal silicide, exposing selected regions of said layer of metal silicide, and developing said selected regions.

90. The method of claim 88, wherein said removing said selected regions comprises etching said selected regions.

91. The method of claim 90, wherein said etching comprises dry etching said selected regions.

92. The method of claim 90, wherein said etching comprises anisotropically etching said selected regions.

93. The method of claim 71, further comprising removing exposed regions of polysilicon through said layer of metal silicide.

94. The method of claim 93, wherein said removing comprises etching said exposed regions.

95. The method of claim 94, wherein said etching comprises dry etching said exposed regions.

96. The method of claim 94, wherein said etching comprises anisotropically etching said exposed regions.

97. The method of claim 93, further comprising removing exposed regions of said layer of insulative material through said layer of polysilicon.

98. The method of claim 97, wherein said removing comprises etching said exposed regions.

99. The method of claim 98, wherein said etching comprises dry etching said exposed regions.

100. The method of claim 98, wherein said removing comprises anisotropically etching said exposed regions.

101. The method of claim 71, further comprising doping at least one source region and at least one drain region of the semiconductor substrate, said at least one source region and said at least one drain region disposable adjacent the gate on opposite sides thereof.